Fall 2015 Firmware Plans

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Features to implement

(In decreasing priority)

Internal pulser (configurable)

- [ ] **Implemented**
- [ ] **Tested**
- [ ] **Merged**

A firmware-emulated pulser designed to replace the external (physical) pulser sitting in the DAQ carts, which acts to limit the rate of triggers from the V1495.

Works by prescaling (slowing down) the internal 100 MHz global clock.

Will have configurable pulse frequency (and pulse duration).

During simulation the pulser has worked, running at the correct frequency; however its pulse length is not configurable yet and the mechanism for limiting matches is unimplemented.

I am currently deciding whether to reserve a detector channel for this internal pulser (permitted by the 32-channel expansion) or emulating its functionality inside the coincidence modules (either by allowing signals through only during the pulser tick or adding an extra condition).

Test suite

- [ ] **Implemented**
- [ ] **Tested**
- [ ] **Merged**

This is meant to exhaustively test new versions of the firmware, to check for essential functionality, edge-case bugs, and performance under stress.

This seems like a two-part plan

Removing intial false trigger

- [ ] **Implemented**
- [ ] **Tested**
- [ ] **Merged**

For the unaware, the V1495 always emits a single trigger within 20 ns after the reset signal (at the

start of a run).

Testing and simulation has revealed that this is caused during initialization of coincidence modules with an empty pattern / mask (i.e. the SPARE unused patterns), when a shift register's slow initialization creates a rising edge signal (which would normally indicate a match).

Several fixes are possible; they include: - Initializing the coincidence modules to a falling-edge, instead of zeroes - Writing a full pattern and empty mask to any SPARE patterns

However, this bug has minimal impact on operations and fixing it will only remove one false trigger.

Version number register

- [x] **Implemented**
- [ ] **Tested**
- [ ] **Merged**

Intended to be read out to operators so they can confirm the firmware binary version and to distinguish development and production builds.

On 8/14/2015 I tested this extensively. I have no clue why this is not working.

Potential bug sources may include mismatched registers in VHDL / XML / C++, or register being read before initialization.

Freezes

Feature Freeze Date: Sept 19, 2015

After this date, no major architectural changes or improvements to the VHDL firmware code, the interfacing C++ code, or XML configuration will be added. Only bug fixes will be permitted from this point forwards.

New features not implemented by this date will not be merged into the master branch, at least until the 2016 summer shutdown.

Work after this date will be solely dedicated to testing functionality and edge cases, as exhaustively as possible.

Code Freeze Date: Sept 26, 2015

After this date, all work on the aforementioned code will cease. Only bugs affecting essential functionality will be fixed from this point on.

Essential functionality includes:

- Trigger efficiency of >90% (triggers fired are <10% smaller than theoretical)
- Correct pattern matching

- Correct timestamps
- Correct register mapping
- Pulse timing / length (veto, delay, triggers)

Essential functionality does not include:

- Cosmetics in configuration parsing
- Internal pulser (easily replaceable by external pulser)
- FIFO output (unless this proves invaluable to fragment reconstruction)

Beamon: ? (Sept 30, 2015)

(Assuming the Fermilab accelerator restart date of Sept 30)

If major bugs persist and cannot be fixed, code should be reverted to one of the following working versions (listed in increasing stability):

- v2.4.0 (trigger_top_J) - internal refactoring (for maintainability)
- v2.2.0 (trigger_top_H) - 32-channel input expansion
- v1.7.0 (trigger_top_G) - the last version of Matthew Stephens' firmware. Used during the Spring 2015 operations.